
The VERITAS Flash ADC Electronics System

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Abstract

The VERITAS-4 atmospheric Čerenkov telescope (ACT) array will employ PMT cameras with high-speed waveform-capture electronics based on 500 Mps Flash Analog to Digital Converters (FADCs). The deep memory of the FADCs provide a true first level array trigger capability that minimizes deadtime and reduces the trigger threshold. An auto-sensing gain switch and a low jitter constant fraction discriminator will minimize the effective FADC gate. This new system will result in a reduction in the energy threshold of the VERITAS-4 array.

1. Introduction

The new generation of imaging ACTs will employ large ($>10\text{m}$ aperture) reflectors viewed by PMT cameras consisting of ~ 300 to 1000 channels. These telescopes will detect electromagnetic showers from gamma rays and reject the cosmic-ray background by performing stereoscopic imaging of the Čerenkov light from air showers. While the technique provides a very large effective area ($\sim 10^5$ times that of satellite experiments) the energy threshold is limited by the small amount of light in the Čerenkov flashes that must be detected against the background fluctuations of the night sky background (NSB). However, Čerenkov signals are intrinsically very fast, with timescales on the order of $\sim 4\text{-}10$ nsec. By using large mirrors, and exploiting the fast timescale of Čerenkov pulses the signal-to-noise ratio (SNR) can be increased.

Poisson fluctuations in the NSB pile up to look like Čerenkov pulses, giving a background that scales like the product of the square root of the pulse integration time τ_G and mirror area A_m . As long as the signal fits within the ADC gate, the signal scales proportional to A_m and does not depend on τ_G . Thus the SNR for event reconstruction $SNR_{\text{reconstruction}} \propto A_m^{1/2} \tau_G^{-1/2}$, and the reconstruction threshold scales as SNR^{-1} . The low time-jitter trigger, dynamically reprogrammable gate and high speed of the VERITAS FADC electronics allow the effective ADC gate to be reduced from ~ 20 nsec to ~ 10 nsec resulting in an improvement in SNR by as much as a factor of $\sqrt{2}$.

Pipelined FADCs can also provide a reduction in trigger threshold. ACTs have typically used gated charge analog-to-digital converters (QADCs) or wave-

form digitizers with their analog inputs delayed to allow time for development of a low-level trigger. The use of FADCs with digital delays (provided by the $8\ \mu\text{sec}$ RAM buffer) eliminates the need for long dispersive delay cables and permits a much longer time for development of an intelligent array trigger.

With conventional triggered ADCs, pulse digitization begins after each local trigger, but is vetoed if no array trigger is forthcoming. The theoretical minimum deadtime associated with this process is twice the signal travel time between the two most widely separated telescopes or about $2\ \mu\text{sec}$. If, for example, the total deadtime for vetoing and resetting acquisition is $10\ \mu\text{sec}$, and the trigger consists of a coincidence of $n = 3$ telescopes then for a 95% livetime one obtains a maximum single telescope trigger rate of $\sim 24\ \text{kHz}$. This limit in rate results in a corresponding limit in the trigger threshold.

Since the accidental trigger rate is a steep function of threshold, a large increase in the maximum allowable rate results in only a small decrease in threshold. The deep memory of the FADC boards, allows the array trigger to act as the first level trigger and common stop for the FADC acquisition. This eliminates the single telescope deadtime limitation. Detailed simulations show that a reduction in trigger threshold of as much as 30% might be realized. The system shows an improvement in both the trigger and reconstruction threshold roughly equivalent to that obtained by increasing the mirror area by $\sim 60\%$

In addition to the reduction in deadtime and improvement in the effective gate, the waveform information from an FADC system contains a wealth of information that can be used to address systematics in energy reconstruction, identify spurious pulses and might eventually be used to improve background rejection. The VERITAS FADCs will also eventually include a dynamically reprogrammable look-back offset and data window allowing special data taking modes to be accommodated.

2. Description of the VERITAS FADC System

The FADC system for the 500 pixel camera on an individual VERITAS telescope will consist of 50 10-channel 9U VME boards distributed in 4 high power VME crates. Each VME crate is equipped with standard CERN v430 monolithic J1/J2 backplanes. The crates also contain a custom clock-trigger board and J3 backplane for synchronous distribution of clock and trigger signals as well as supplemental power for the 150 Watt modules. To date, 25 boards and two FADC crates have been produced for the prototype VERITAS telescope.

Figure 1 shows a schematic of the system. The analog signal from the PMT is fed to a shaping amplifier and then fanned out to the FADC and to the CFD circuits. The boards digitize each PMT signal at a 500 Msp/s rate depositing the result into a circular RAM of depth $8\ \mu\text{s}$. This continues until the Level 3 (Array) Trigger stops digitization and initiates the acquisition process. When

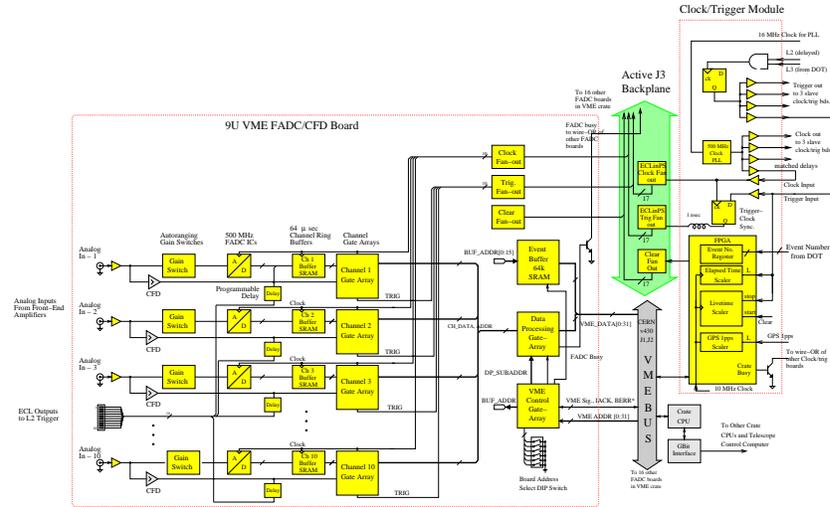


Fig. 1. Schematic of VERITAS FADC system.

the array trigger arrives, the memory contents of all channels are simultaneously examined for the presence of a signal above a zero suppression threshold. Data from all channels above threshold are formatted into an on-board buffer RAM, awaiting VME read commands. After each FADC board in a crate releases the busy signal, the VME CPU initiates an A32/D32 chained block transfer (CBLT), a type of DMA transfer designed to handle variable length data distributed over a number of modules.

Data is read from the first to the last board using a chained block transfer. This is accomplished by a token that is passed from one board to the next through the IACK daisy chain as each board empties its buffer. When the last board finishes, it terminates the transfer by issuing a BERR* signal. Tests of the full acquisition system show 10 MB/sec data rates. We estimate the data rate to be 2 MBytes/sec/telescope, so our system should be more than adequate for operation up to kHz array trigger rates.

The FADC effectively has a method for looking backward in time up to $8\mu\text{s}$ to locate the stored digitized signal to the nearest 2 nsec sample. The jitter in the leading edge time of pulses with 4nsec rise time was measured to be better than $\sigma_t = 0.62$ nsec on all channels of the prototype electronics. Using the CFDs as a self-trigger, we have achieved time jitter of ≈ 1 nsec for Čerenkov pulses.

The programmable look-back offset and data width allow the exact pulse location for each channel to be ‘re-tuned’ in later analysis using calibration pulses from an optical pulser that simultaneously illuminates the PMTs and using the event data itself, allowing real-time calibration of the signal propagation times. Together with the very low time-jitter, this allows the effective gate for charge integration to be kept to the minimum value.

To achieve a large dynamic range, our design includes an autoranging gain

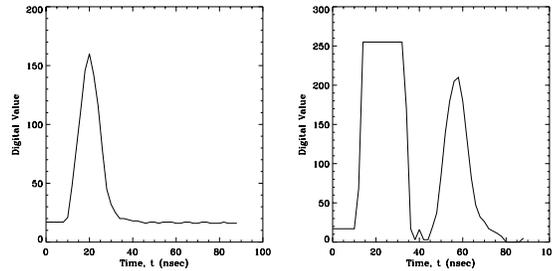


Fig. 2. Pulses recorded with an FADC board (a) below the gain-switch threshold, (b) above the gain-switch threshold.

switch to extend the dynamic range from 256 to 1500. An analog switch normally connects the high gain channel to the FADC integrated circuit, but when the signal exceeds threshold the switch is thrown and connects the delayed low gain channel instead. This produces a scaled pulse following the truncated saturated pulse (see Figure 2). The intrinsic noise floor on the FADCs, determined from the pedestal variance, has been measured to be $\sigma_{\text{pedestal}} = 0.50 \pm 0.18$ digital counts (at high gain) for the prototype boards. With the addition of the CFD daughterboards, the noise stays below $\sigma = 1$ d.c. on all channels. The dynamic range is thus 1500:1 or 750 photoelectrons when the gain is set to 2 d.c./p.e. When a channel is presented with a maximum amplitude pulse, crosstalk on adjacent channels is not measurable (< 1 d.c.).

Incorporating the CFDs on the FADC board simplifies the signal fan-out and eliminates the need to duplicate the VME interface. It also provides the ability to register the *triggering* discriminator hit patterns at rates up to 120 MHz. These bits accompany the corresponding FADC words in the RAM, and provide a buffered record of the CFD output states. The CFD threshold and output width are programmed via a serial data link from the FADC board interface gate arrays. The output of the CFD board is fanned out to a 40 MHz singles rate scaler on the FADC board and to a programmable ECL delay with 750 psec resolution. This delay allows the CFD pulses to be matched at the FADC front-panel output to better than 1 nsec. The minimum CFD output pulse width of 5 nsec together with the ability to dynamically realign the trigger pulses allows the coincidence resolving time to be minimized.

Custom clock/trigger boards synchronously distribute the array trigger, a common clear used to restart acquisition, and a common 500 MHz clock. The clock/trigger boards also provide scalars for latching the event time and livetime. The master clock/trigger board provides a synchronous clock to each slave board which is used to phase-lock the 500 MHz clock.*

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