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## The Zero-Degree Detector System

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James H. Adams, Jr.<sup>1</sup>, and Evgueni Kouznetsov<sup>2</sup>

(1) NASA Marshall Space Flight Center, Huntsville, AL 35812 USA

(2) University of Alabama in Huntsville, Huntsville, AL 35806 USA

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### Abstract

A new detector system has been developed to measure light fragments from heavy ion fragmentation reactions. The detector system separately measures the signals from simultaneous fragments.

### 1. Introduction

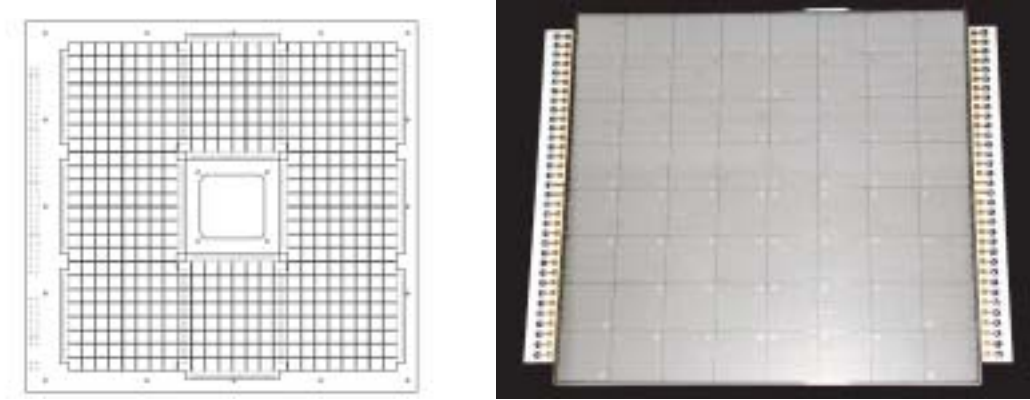
This detector system is intended to measure production cross sections for fragments from heavy ion collisions. In conventional experimental arrangements large monolithic detectors are used. Because of signal pile up with these detectors, it is not possible to reliably reconstruct the contributions of the light fragments. The solution is to separately measure the signal of each fragment so they can be identified. To do this we use a system of highly segmented detectors, the Zero-Degree Detector System. This system individually identifies multiple light fragments near the beam by measuring each fragment in a separate two-element charged particle telescope.

### 2. Concept

The detector system consists of 1-cm<sup>2</sup> silicon charge particle telescopes, each with two elements. These telescopes are arranged in a ring surrounding the beam as shown in Fig. 1a. Each fragment that strikes this ring will penetrate two detectors and be measured twice. This creates a coincidence so noise signals will not be mistaken for lightly ionizing fragments. Combining the two measurements of each fragment also reduces the error on the charge measurement by  $\sqrt{2}$ .

Each detector layer consists of 64-pad silicon detectors. Between the first and second layer the fragments will pass through the 760  $\mu\text{m}$  ceramic card below the first detectors and a 1.57 mm printed circuit board that carries the detector units. This intervening material will help to de-correlate the knock-on electron production so the measurements made in the two detector layers will be statistically independent.

The detector system is configured as a ring to avoid damage from accelera-



**Fig. 1.** (a) Zero Degree Detector (left) and (b) 64-pad detector card.

tor beam particles that do not interact in the target while detecting particles that have little transverse momentum and are only slightly deflected from the beam.

### 3. Detector Unit Design

The detectors are made Micron Semiconductor, Ltd.[4] on the  $300\ \mu\text{m}$  thick 6-inch polished wafers of high resistance ( $R > 5\ \text{k}\Omega\text{-cm}$ ) float zone phosphorous-doped silicon. On each wafer a square matrix of 64 pads is made on the rectifying contact side. The overall dimensions of the detector are  $83 \times 83\ \text{mm}$ . Common guard rings occupy the space around the 64-pad array. A passivation layer protects the surface of the detector. This layer has small windows on each of 64 pads to route signals. The opposite (blocking contact) side of the detector unit has a gold coating to ensure good contact to conductive adhesive.

### 4. Detector Card Design

Each detector unit is mounted on a ceramic substrate to provide mechanical support and electrical connections from the detector pads to the front-end electronics (see Fig. 1b). These substrates ( $7.3 \times 11.3\ \text{cm}^2$  and  $0.76\ \text{mm}$  thick) are made from  $\text{Al}_2\text{O}_3$ . Each substrate has a printed circuit made from the gold paste deposited on the surface of the ceramic to make the connection to the blocking contact side of the detector. Along opposite sides of each substrate are two rows of 34 pins. Two middle pins in each row connect to the blocking contact side of the detector, which is attached to the printed circuit and the substrate with silver filled conductive adhesive. The other 32 pins in each row are connected to nearby pads, which are also printed on the substrate. These pads are used for wire bonding to the detector. The rows of pins plug into the motherboards.

## 5. Routing of signals from detector pixels

The signals are routed from the detector pads to readout circuitry over the passivation on top of the detector pads. After the passivation of the detector surface on the rectifying contact side by  $\text{SiO}_2$ , additional aluminum traces with pads for wire bonding are deposited on top of the passivation. Afterwards the traces are also passivated. Traces electrically connect to individual detector pads, through the small windows in passivation mentioned above, with two rows of small bonding pads that are deposited near opposite edges of detector. When the detector is mounted onto ceramic substrate, these pads are near corresponding bonding pads on the substrate. Wire bonds are now made between the detector and the substrate to complete the connections of the signals to the pins. To avoid this cross talk between channels, the capacitance between traces and pads they cross is kept small by making the thickness of the passivation as large as possible and width of traces as small as possible. In this design one must also be concerned with the electrical resistance of the traces connecting the pads to the pins. It must be  $<20$  ohms. The maximum thickness of the aluminum traces made with standard technology is  $1.2 \mu\text{m}$ . To keep resistance of the traces small, the width of trace must be adjusted. The resistance of a trace with  $1.2 \mu\text{m}$  thickness is given by:

$$R = 220/WL$$

(in ohms), where  $W$  is the trace width ( $\mu\text{m}$ ) and  $L$  is trace length (cm). The longest traces are 3.5 cm. For these traces to have a resistance of 20 ohms, the trace width must be  $39 \mu\text{m}$ . That gives us a capacitance 5.0 pF to the pad at the edge of the detector, including bonding pad capacitance.

The cross talk due to this capacitance was simulated using hardware from the Advanced Thin Ionization Calorimeter (ATIC) cosmic ray experiment[1] that uses the same front-end electronics as the Zero Degree Detector. 56 pF capacitors were connected to two channels to simulate the capacitance of the  $1\text{-cm}^2$  pads. A 10 pF capacitor was connected between the channel to simulate the stray capacitance between the trace and the detector. A signal was injected into one channel and the cross talk was observed on the other. The cross talk was measured to be  $+0.07\%$  with a safety margin of 2, which is acceptable for our applications..

## 6. Readout Electronics

The readout electronics, based on the design used in ATIC experiment[1,3]. One silicon layer comprises 8 silicon detectors or 512 channels. 32 CR1.4 chips[2] will read out all these channels. 8 chips will be connected in one daisy chain so 4 groups of 8 CR1.4 chips will shift out analog information in four output streams. 8 silicon detectors on substrates will be plugged into one motherboard so that 6

detector cards will be located on one level and two cards will be raised by 0.8-1.0 mm to allow overlapping.

The side of the motherboard opposite the detector cards carries the front-end electronics. We will use 32 CR1.4 ASIC chips with biasing and calibration circuitry, analog drivers and control logic. Analog information from all detector pads comes serially in four streams to the Grandmother board (GMB). The GMB design is based on a similar board used in the ATIC project. The GMB has 5 analog input channels and 5 16-bit ADCs (providing one spare stream). It also contains transceivers for connection to the following ASIC Control Logic Board (ACLB), a calibration pulse generator based on a 16-bit DAC, analog drivers and control logic for distributing of control signals for CR1.4 chips to the 5 streams. Analog signals from the motherboard are digitized and serially go in four streams of digital signals to ACLB. ACLB contains 2 field-programmable gate array (FPGA) chips. One of them supports communication protocol with a custom computer interface card (Digital Interface Module or DIM) and provides on-line sparsification of the readout data. Second FPGA chip generates control signals for the CR1.4 chips, the calibration DAC and controls digitization process of GMB. Additionally it has transceivers for communication with the GMB and trigger circuitry with an adjustable delay for the Track/Hold signals that are routed to the CR1.4 chips. This trigger comes from a beam line trigger scintillator and is delayed so that the Track/Hold signal occurs at the peak of the shaped output signals in the CR-1 chips. DIM card plugs into a computer ISA-bus to support a custom communication protocol with the ACLB.

The ACLB and DIM cards will be used the same way as they were used in the ATIC project and all communication protocols will be the same therefore readout time of the full system for one event is 1140  $\mu$ s.

## 7. References

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4. Micron Semiconductor Limited, 1 Royal Buildings, Marlborough Road, Lancing, Sussex, BN15 8UN, UK (<http://www.micronsemiconductor.co.uk/>).