The ToF and Trigger Electronics of the PAMELA Experiment

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Abstract

The electronics of the Time of Flight telescope [1] and the trigger of PAMELA experiment [2] are described. The time resolution requested by the ToF system must be less than 120 ps. The contribution of the digitization electronics is negligible if the TDC resolution is ≤ 50 ps. The peculiarity of the developed electronics arises from the need to obtain such a time resolution associated to a wide dynamic range for charge measurements, operating in a satellite environment, which implies low power consumption, radiation hardness, redundancy and high reliability.

1. Introduction

The PAMELA ToF - Trigger electronics is a system composed by nine 6U VME boards. As shown in Fig. 1. six Front End boards (FE) performs the time and charge digitization of the 48 PMTs pulse of the PAMELA ToF. Data from these are collected by a DSP board through serial links and, after digital processing, transferred to the main data acquisition system. Finally the Trigger board receives signals from FE boards to generate the main trigger to the apparatus, handles the busy logic of all the subsystem and with the aid of about 60 rate counters allows the monitoring of the ToF and other subsystems performances.

2. The Front-End board

The FE boards, Fig. 2., receive the analog signals from PMTs, 8 for each board. For each channel it measures the arrival time of the signal with respect to the trigger pulse and its charge and generates the signals for the trigger. The PMT signal is split into two branches at the input stage to measure time and charge.

2.1. Time section

Each PMT anode is coupled to a fast discriminator. To minimize the time-walk effect a double threshold discriminator is used. The chosen comparator is

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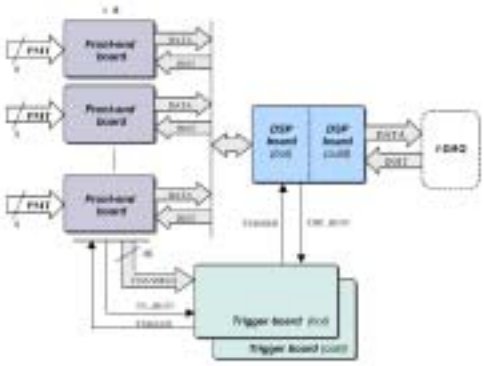

Fig. 1. General electronics layout

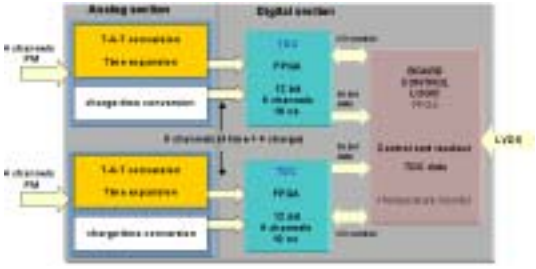

Fig. 2. Block diagram of the Front End board

the AD8611 that has a maximum propagation delay of 4 ns. The two thresholds of the comparators are settable by remote through two DAC AD 7303. The discriminated signals are shaped, translated in LVDS standard and sent to the trigger board. The discriminator is part of a more complex logic that controls a double ramp Time-Amplitude-Time (TAT) converter. A low loss, low thermal drift storage capacitor is charged with a high stability constant current source during the time between the pulse edges of the front-end discriminator and the trigger signal. The arrival of the trigger signal starts the discharging of the capacitor with a constant current that is about 200 times smaller then the previous. In such a way, measuring the discharging time, a time expansion factor of 200 is obtained. All the propagation delays in start and stop sections are matched. A fast discharge is produced if the trigger is not generated within 150 ns from the signal edge. All the logic needed to control the TAT converter is fully implemented in a low-power, rad-tolerant Actel 54SX08A FPGA. Each of these devices serves two channels so a total a four FPGAs are present on the board.

2.2. Charge section

The amplitude of each PMT pulse is measured with a Charge-to-Time converter. A charge amplifier collects the anode current of the PMT signal and provides an output signal proportional to the total current. A pulse stretcher operates by charging-up a capacitor at the peak value of the input waveform and then discharges it linearly. This signal has a length proportional to the maximum voltage reached on the capacitor and hence to the PMT charge. The charge amplifier and the pulse stretcher are implemented using the monolithic transistor array CA3127, manufactured by Intersil. The five transistors of the array have a value of f_T in excess of 1 GHz, low 1/f noise and are at the same temperature. The last stage of the Charge-Time converter is a discriminator that generates the digital pulse with a length equal to discharging time of the pulse stretcher.

2.3. Digital section

The digital signal obtained measuring the discharge time of capacitor, coming from time or charge section, is sent to a 100 MHz TDC fully implemented in a Actel 54SX32A FPGA. This TDC is a multichannel, common start time-to-digital converter, with 8 channels per chip. The time measurement is done digitally by counting 100 MHz clock periods generated by an external quartz. The circuit has a 10 ns resolution over a time window of 40.95 μs, which means a 50 ps resolution on a range of 200 ns, taking into account the time expansion factor. The circuit is realized with a 12 bits Gray counter and 8 registers. The first edge of trigger signal starts the counting of the counter and when a new signal edge is presented at one of the channel inputs, the hit control logic write the current value of the free running counter in the its own register. The registers are 16 bits long (12 + 4) to code the channel number.

Each TDC receives a signal for measuring the time and one for the charge for each channel so the board houses two TDC. The readout and the initialization of the TDCs is performed by a dedicated 54SX32A FPGA which is the interface between the ToF and the DSP boards. Under request of the DSP board it acquire data from the two TDC and writes it in a 16 hits deep FIFO. The data are then serialized and transmitted according the Data-Strobe protocol at 16 Mbit/s. The total power dissipation of the board is less then 3 W.

3. The DSP board

All the PAMELA data read-out is performed through a Data-Strobe serial link and each subsystem has a dedicate link. To readout the six FE boards of the ToF subsystem an interface DSP board has been developed which collects data from the six boards and transmit it, through the serial link, to the main DAQ. On this boards is present a Digital Signal Processor (Analog Device) ADSP 2187L which collects data and built the data packet for the main acquisition. An Actel 54SX32A FPGA contains all the state machines needed to decode macro-commands from CPU and to control the interface with DSP, a second Actel controls the data flow with the FE boards. As shown in Fig. 3. on the same VME board two copies of the circuit are implemented. To increase the reliability of the system this board has a 'cold' version that can be turned on in case of failures of the 'hot' one preserving the full functionality of the system.

4. The trigger board

The trigger board is a complex digital board that generates the first level trigger for the apparatus and performs several more tasks. It receives the 48 signals from ToF system for the main trigger and about 8 signals from other subsystems able to generate autotrigger for particular events. To guarantee synchro-

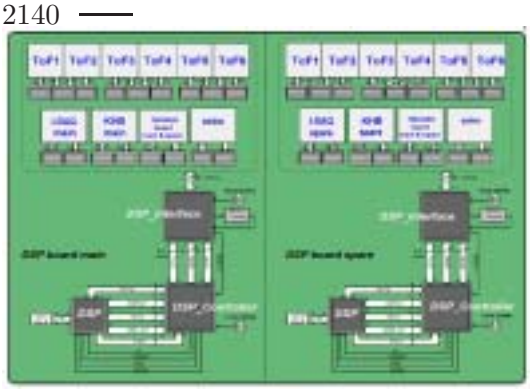

Fig. 3. A block diagram of the DSP board

Fig. 4. The trigger board

nization of the data acquisition the trigger board manages the busy lines coming from each of the PAMELA subsystem for a total of 20 busy line. All the input and output lines are in the LVDS standard. About 60 rate counters, dead-live time counters and the logic to generate calibration pulses sequence for different subsystem of the apparatus are also implemented on the board. The logic is distributed on 9 Actel 54SX32A FPGAs as shown in Fig. 4. Control masks select trigger types and allows the selection of failed (noisy or dead) ToF channels. The pattern of the channels fired for each trigger is generated for each event. A DSP (ADSP 2187L) is used to manage the data structure organization and to monitor the rate counters of the ToF channels and other subsystems.

5. The performances

The first test of the performances of the ToF electronics has been performed on the engineering model of the FE board. Time resolution and integral non linearity have been measured with an AGILENT 81132 pulse generator (RMS jitter of the time base = 15 ps ± 0.001 % of the delay). In Fig. 5. the result of the two measurements are shown.

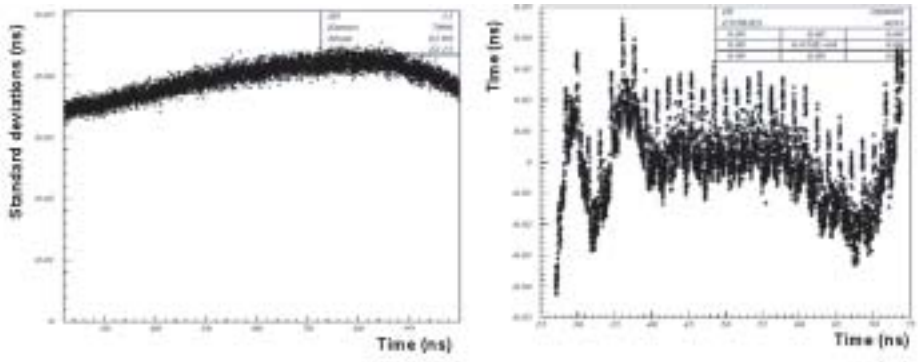

Fig. 5. The time resolution and the integral non linearity measurement results

6. References

1. Campana D. et al., proceedings of this conference.
2. Simon M. et al, proceedings of this conference.