Environmental Testing of the Front-End Electronics for the Auger Observatory Surface Detector

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Abstract

The Pierre Auger Observatory Surface Array uses mixed analog/digital low noise electronics for the detection of the highest energy cosmic rays. The southern site, which has a targeted operational life of 20 years, contains 1600 stations spread over 3000 km^2 of difficult to access terrain with a wide range of local temperatures. The production of a very large outdoor array necessitates a quality assurance plan. This includes both functional testing of the electronics to verify compliance with specification and environmental stress screening ranging from $-20°$C to $70°$C. The production test rig, testing procedures and performance of the front-end electronics will be discussed.

1. Introduction

The Front-End (FE) electronics of the Auger Observatory surface array are being integrated with the rest of the Surface Detectors (SD) [3]. Twenty years of temperature variation will cause wear on the electronics, and a small support staff must maintain the numerous stations over a huge area. Thus, testing is important to keep the mean time between failures in the field low.

2. Procedures

The FE accepts analog signals from the photomultiplier bases, filters those signals before digitizing them in 40 MHz ADCs, analyzes the digitized signals for interesting trigger patterns using Programmable Logic Devices (PLDs), and communicates with the Unified Board (UB) PowerPC® 403GCX (PPC) based detector station controller. The testing procedures are designed keeping the mixed analog/digital nature of the FE in mind. Testing begins with a simple "smoke test" in which the quiescent supply currents are measured in an over-current protected test fixture. This test protects the rest of our test apparatus from catastrophic failures. The testing then proceeds to Environmental Stress Screening (ESS) and Functional Testing (FT). If at any stage a FE is nonconforming,

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(a) (b) (c)

Fig. 1. (a) ESS test board with one of the FE boards connected. The place for another FE board is left empty. (b) A picture of the ESS test rig, its closed environmental chamber at the top and electronics, which include data acquisition modules and regulated power supplies, at the bottom. (c) A picture of the FT rig. The UB is inside the environmental chamber with the FE board under test connected.

then it is removed and segregated until it's reworked and tested again [1].

2.1. Environmental Stress Screening

Two FE boards are connected to each of eight ESS test rig boards for insertion into an Environmental Chamber (EC) (Fig. 1a,b); this yields a throughput of 16 FE boards in two days. The EC is cycled between +70°C and −20°C. The ramps between the extremes are accomplished in 60 minutes per transit and the extremes are held for 30 minutes each [2]. The tests, executed during the 30 minute hold time, include power cycling, loading of config file(s) into the PLD(s), setting the analog input, writing to registers, sending triggers and observing outputs. Supply currents are continuously monitored. This is all automated (Fig. 2a). At 25 hours, EC has been ramped to +70°C and is held for 20 hours.

2.2. Functional Testing

The FE board is connected to the UB and placed into a different EC (Fig. 1c) for the functional testing. Functional testing is repeated at +70°C, −20°C and +25°C. The UB loads a config file into the PLD(s), writes/reads from each PLD register and configures the FE board trigger. Test pulse patterns from an Arbitrary Waveform Generator (AWG) are sent into the six analog inputs, two channels at a time (one "low gain", one "high gain"). The shower and muon buffers are read out to verify timing and trigger patterns, and to measure gain, pedestals and cross talk (Fig. 2b).

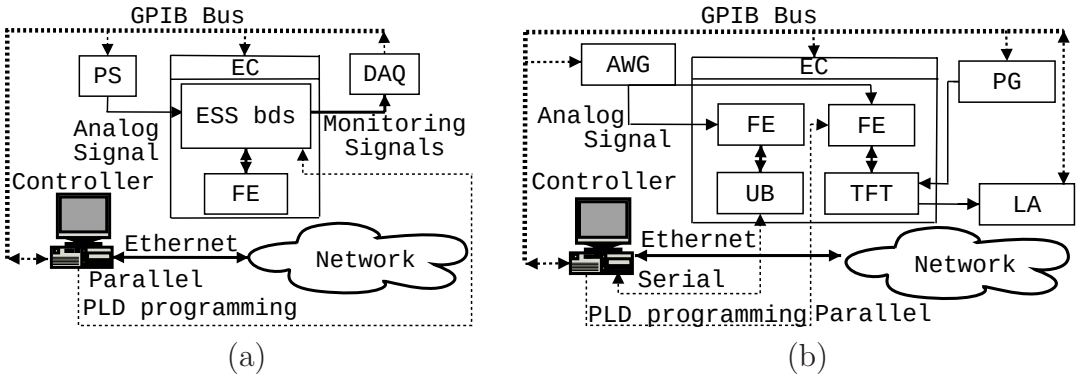

Fig. 2. Block diagram of ESS Rig (a) and Functional Test Rig (b).

3. Hardware

Test rigs combining commercial and custom-designed electronic devices were created in order to realize the procedure.

3.1. Environmental Stress Screening Test Rig

The ESS rig (Fig. 2a) consists of: ESS Test Boards (Fig. 1a) - custom boards that route test signals to and from the FE board, provide for the PLD programming, supply a clock signal to the FE board and measure the supply currents of each tested FE board; EC (Fig. 1b) - GPIB controlled temperature chamber, which holds eight ESS test boards, used for the temperature cycling; Power Supplies (PS) - GPIB controlled supplies that drive the FE analog inputs; Data Acquisition Module - GPIB controlled unit that monitors the signals from the ESS test boards.

3.2. Functional Test Rig

The FT rig (Fig. 2b) consists of: EC (Fig. 1c) - GPIB controlled temperature chamber; UB - standard Auger station controller linked to control PC via a serial cable; Sacrificial Board - a custom board that prevents wear out of the UB to the FE connectors because of multiple FE insertions; AWG - GPIB controlled wave generator that produces signals for the FE analog inputs; RF Mux - GPIB controlled RF switch that sends AWG signals to two of six FE inputs.

3.3. Timing Function Test Rig

The Timing Function Test (TFT) rig consists of: EC - the same device that is used for the FT; Pattern Generator (PG) - GPIB controlled unit that provides stimulus to the FE, 24 bit test vectors at 250 MHz; Logic Analyzer (LA) - GPIB controlled unit which records the response to stimulus; TFT Board -

custom board that performs routing of the signals from the PG to the FE board to be tested and from FE board to the LA.

4. Software

A number of software packages were developed to automate the testing.

4.1. GPIB under Linux® Access Software System (GLASS)

GLASS accesses multiple GPIB devices using standard C^{++} functions. GPIB devices can be accessed from any computer connected to the same network as the controller PC. The address of GPIB device is a mix of the IP address of the controller PC and the device's number in the GPIB network.

4.2. Front-End Electronics Tester (FEET)

FEET was created as a straight-forward implementation of the testing procedures described above. It's based on the GLASS and ROOT© [4] packages and written in C^{++}. Devices which participate in the tests are controlled by GLASS. Results of each test are recorded in the database, FEETDB, according to the serial numbers of the tested board. FEETDB is organized in a such way that results can be accessed in HTML format.

5. Status

Initial batches have gone through testing. Estimates of our front-end board test procedures indicate that they are appropriate to remove infant mortality and avoid wear out.

6. Acknowledgments

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7. References

1. Blowers J., 2001, *Pierre Auger Observatory Quality Assurance Plan*, EDMS Id:307141 v.3.
2. Clark P. and Dye A., 2002, GAP-2002-002.
3. Szadkowski Z. *et al., for the Pierre Auger Collaboration 2003, The Surface Detector Trigger for the Auger Observatory, Contribution to this conference.*
4. *http://root.cern.ch/*