A Proposal Of A Single Chip Surface Detector Trigger Based On Altera Cyclone^{TM} Family

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Abstract

In May 2003 the new Altera® PLD family Cyclone^{TM} appears on the market. The new chip allows significantly simplifying the construction of the surface detector trigger as well as decreasing the total costs and improving parameters. In comparison with currently approved ACEX® chips, Cyclone chips contain much bigger internal memory (a possibility of implementation of slow memory inside the PLD chip or extension of fast buffers). 1.5 V supplies the core (reduction of power consumption). The single chip allows implementing interleaving DMA mode and avoiding problems with chips synchronization. The register performance indicated by compiler is on the level 130 MHz. Such a high internal speed allows increasing the sampling frequency, which could improve a time resolution of the trigger. More resources allow implementing new kind of triggers based upon Power Spectrum Density. MegaCore® library offers DSP routies as FFT, which may be useful to recognize type of events.

1. History

The general structure and functionality of the trigger/memory circuit has been described in [3]. The works on the Trigger/Memory Circuit (TMC) started since 1998, planned originally as an ASIC [1], containing all functions in the single chip, together with the memories for the fast and slow channels. The dynamically development of the Programmable Logic Devices (PLD) allowed implementing sophisticated algorithms into PLDs avoiding possible risk, if some bugs in ASIC code were not found. Reprogramming in the circuit gave additional advantage of adding new or modifying old routines, of adding new features developing on collected data [5]. The parallel path of PLD development started in March 2000 used the Altera EP20k200RI240-2 PLD from the APEX family [6]. The capacity of internal memory allowed implementing fully fast channel into PLD chip (2 buffers per 64-bits 768 words). The slow memory had to be added externally as Dual-Port RAM IDT70V3569S6DRI. First TMC based on APEX PLD solution started to be installed on the Auger Engineering Array since December 2000. All

data registered up to now (May 2003) in the Auger Experiment are due to APEX trigger PLD solution. The only disadvantage of that trigger is the cost of PLD. Since December 2001 the new cost effective solution based on the new Altera EP1k100QI208-2 chip from the ACEX family has been developed and in June 2002 has been approved as the baseline for all Auger Surface Detector Electronics [8]. Simultaneously ASIC path has been terminated [4]. ACEX family reduces significantly the total cost (300k$ for all tanks), however due to smaller internal memory required an implementation of two PLDs working synchronously and parallel.

2.   Chips resources

Family	Chip	LE	Memory bits	PLD chips	Mem chips	PLD cost	Mem cost
ASIC				1	0	>100$	-
APEX	EP20k200RI240	8320	106 496	1	1	290$	60$
ACEX	EP1k100QI208	4992	49 152	2	1	120$	60$
Cyclone	EP1C12Q240	12 060	239 616	1	1	125$	60$
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The ASIC design would be the most cost effective and the simplest solution. However, due to the fixed algorithm implemented in the silicon structure, future modification of the code is not possible. The experiences from the Engineering Array confirmed that the flexibility in the code modification is necessary. On the beginning some very rarely possible configuration have not been taken into account and caused data integrity violation [6]. Also adjustment of the interruption pulses length allowed avoided possible conflicts with GPS module. The single chip of TMC would be the best solution due to high reliability important in long-term working system. The APEX design working perfectly on the Engineering Array has unfortunately the one significant disadvantage - the price of PLD chip. The total cost of TMC far exceeded the assumed budget was the reason of looking for more cost effective solution without any functionality reduction. The APEX chip allowed implementing fully fast buffers into internal PLD memory. The slow buffer was implemented as the external Dual-Port RAM. The new cost-effective ACEX family offered the inexpensive chips with sufficient resources of logic elements, but unfortunately not sufficient internal memory. The signal path has to be split into two parallel paths performing synchronously. Two ACEX chips were enough to perform all APEX tasks. The high gain fast channel was performed by ACEX_A, the low-gain fast channel by ACEX_B respectively. The slow channel remained almost the same and has been implemented into ACEX_A. Triggers were generated from only 30-bits of high-gain channel in ACEX_A and next were transferred by additional I/O chain to ACEX_B to synchronously record

data for low-gain channel. Additional I/O chain is necessary to reduce an influence of propagation times from inside the chip to the chip pins and next to the internal structure of the next chip. However such a two chips design requires additional mechanism of synchronization. Some parts of code have to be duplicated in adjacent chip.

3. Cyclone design

The new Altera family Cyclone available since May 2003 offers chips with much higher capacity of resources and memories. EP1C12Q240C7 chip allows implementing all function of both fast and slow channel into single chip. Up to now two variants of the AHDL code have been prepared: a) with the Dual-Port RAM for slow channel as in the current design, fast channel implemented into PLD Cyclone as in APEX design, b) single chip design, both channels implemented in the Cyclone chip [9]. The not yet used memory block implemented as FIFO for slow memory buffers. The size not previously used memory block allows implementing only 3584 word 32-bit FIFO for the slow channel. The external Dual-Port memory offers 2 buffers per 8192 32-bit words, but it seems to be overkill. 3584 words is sufficient.

Variant	LE	Memory bits	f_{max}	PLL	I/O
DP_RAM	4325 — 35%	98 304 — 41%	177 MHz	2/2	164
Single chip	4460 — 36%	212 992 — 88%	130 MHz	0/2	113

The free resources give an opportunity of adding new functions. One of them is the new type of trigger based on Power Spectrum Density (PSD) [2]. The current used triggers require relative small resources. PSD requires much more, depending on the length of window and resolution. PSD trigger should distinguish events with pedestals from pure spikes. Time over threshold trigger (ToT) [6] for medium threshold may not distinguish events with relative high pedestal and short spikes. Energy related to "pedestal" events is higher than for pure short spikes and may be the better estimator than ToT trigger. The next direction, which started to be investigated, is the spectral analyses of events. Altera® offers Digital Signal Processing library of routines like Fast Fourier Transform, which may be useful with recognition of events almost online. Preliminary analysis of registered over 4000 events on Engineering Array allows adjusting additional most efficient tools supporting by hardware triggers.

4. Advantages of Cyclone design

Reliability increasing of the whole trigger and significantly simplifying of the board. No problems with chips synchronization (as in current design with ACEXs). Available both non-interleaving and interleaving DMA modes. No

change of micro-controller software for non-interleaving mode (as in APEX). Better flexibility for a design optimization due to more Cyclone's resources than two ACEX chips. 1.5 V (instead of 2.5 V as in ACEX) supply of the core of Cyclone chip, reduction of power consumption by factor 2.5. 2 PLLs for future optimization (up to 0.01 ns shift grid). Plastic Quad Flat Pack 240 pins (as in APEX design), for EP1C12Q240. Very high internal register performance (130 - 170 MHz), possible increasing of sampling frequency for ADC to 80 MHz with faster ADC like AD9214. The Cyclone cost for the single chip design (40 MHz) less than for ACEX one. Possible new triggers based upon Power Spectrum Density. Possible implementation of routines from MegaCore® library for Digital Signal Processing as for example Fast Fourier Transform. Quartus® II compiler v.2.2 provides the second synthesis pass much better optimizing timing.

5.   Acknowledgments

6.   References

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